

CMOS MAPS development for Belle II vertex detector upgrade -- OBELIX sensor for VTX project --

Katsuro Nakamura (KEK) Mar 29, 2024 研究会「EICで展開する新たな原子核・素粒子物理」

CMOS Monolithic active pixel sensors (MAPS)

Monolithic Active Pixel Sensor (MAPS) based on CMOS imaging processes

- Sensor: the epitaxial silicon layer grown on low-cost and low-ohmic substrate wafers
- Monolithic: full CMOS circuitry integrated into active area and periphery
- Because in standard CMOS technologies the allowed biasing voltages and epi-material resistivity are low, the depleted region is localized around the electrode.
- \rightarrow Charge collection mainly by **diffusion** : slow and incomplete collection was bottleneck.
- Successfully used in lower hit rate and radiation level than LHC(p-p), like STAR and ALICE.
 - NIEL < $10^{13} n_{eq}/cm^2$



Depleted Monolithic Active Pixel Sensor (DMAPS)

Depleted CMOS MAPS

- Improved CMOS technologies utilize high resistivity depleted silicon layers to achieve a depletion region underneath the collection electrode (typically about 20um)
- Charge collection by **drift** : Fast (~10ns) and efficient charge collection
- Small collection electrode: Small noise and low power consumption due to small C_{det}
- Low-dose n layer: full depletion with uniform electric field
- \rightarrow High hit rate and radiation environment tolerance
 - NIEL ~ $10^{15} n_{eq}/cm^2$ is achievable.



Belle II Vertex Detector Upgrade

- New vertex detector VTX: Fully pixelated 5-layer detector, using CMOS MAPS
 - Higher space-time granularity
 - Small material budget: about 2.4%X₀
- Target installation timescale is LS2 for SuperKEKB machine upgrade.
 - Still, detailed plans for LS2 are under discussion
- Thin DMAPS sensor: Optimized BELle II pIXel (OBELIX) chip
 - New sensor for Belle II vertex upgrade
 - TowerJazz 180nm
- OBELIX matrix design is based on TJ-Monopix2 for HL-LHC ATLAS
 - Implementing new digital periphery and trigger logic for Belle II
 - Detailed performance characterization of TJ-Monopix2 is crucial for OBELIX design



VTX project: DMAPS development for Belle II upgrade

Solid

state

Vertex detector²⁾



VTX collaboration

HEPHY (Vienna) CPPM (Marseille) IJCLab (Orsay) IPHC (Strasbourg) University of Bonn University of Dortmund University of Goettingen KIT (Karlsruhe) KEK (Tsukuba) University of Tokyo IPMU (Kashiwa) University of Bergamo INFN & University of Pisa INFN Pavia IFAE (Barcelona) IMB-CNM-CSIC (Barcelona) IFCA (CSIC-UC) Santander IMSE-CNM-CSIC (Seville) IFIC (CSIC-UV) Valencia ITAINNOVA (Zaragoza) QMU (London)

MAPS in the ECFA Roadmap (DRDT3.1)

- Identified as critical to achieve the science program outlined in European Strategy for Particle Physics
- DRDT 3.1
 Achieve full integration of sensing and microelectronics in monolithic CMOS pixel sensors

 DRDT 3.2
 Develop solid state sensors with 4D-capabilities for tracking and

calorimetry DRDT 3.3 Extend capabilities of solid state sensors to operate at extreme fluences

DRDT 3.4 Develop full 3D-interconnection technologies for solid state devices in particle physics





	DRDT	
Position precision	3.1,3.4	
Low X/X _o	3.1,3.4	
Low power	3.1,3.4	
High rates	3.1,3.4	
Large area wafers ³⁾	3.1,3.4	
Ultrafast timing4)	3.2	
Radiation tolerance NIEL	3.3	
Radiation tolerance TID	3.3	



< 2030

Requirements for the VXD upgrade

Targets

Radius range	14 – 135 mm		
Tracking & Vertexing performance at least as good as current VXD			
Single point resolution	< 15 um		
Material budget per layer	~0.2% X ₀ (inner), ~0.8% X ₀ (outer)		
Hit time resolution	< 100 ns		
Robustness against radiation environment current extrapolation with safety factor x5			
Hit rate ^(*)	~ 120 MHz/cm ²		
Total Ionizing Dose ^(*)	~ 0.1 MGy/year		
NIEL fluence ^(*)	$\sim 5.0 \times 10^{13} \text{ n}_{eq}/\text{cm}^2/\text{year}$		

(*) requirement for the innermost layer (R=14mm)

Required hit rate tolerance vs. Radius



Possible other improvements by upgrade

- Impact parameter resolution
- Tracking performance for low- p_{T} tracks
- Longer trigger latency
- Capability of Level-1 trigger creation

TowerJuzz Monopix-2 (TJ-Monopix2)



TJ-Monopix2 sensor: developed for HL-ATLAS

- DOI: 10.1016/j.nima.2020.164403
- 7-bit ToT, 3-bit in-pixel threshold tuning
- Column-drain read-out inherited from ATLAS FE-I3
- Detection efficiency assessed up to 10¹⁵ neq/cm²



TJ-Monopix2 Performance Characterization

TJ-Monopix2 sensor



Detailed performance characterization of TJ-Monopix2

- Laboratory testbench test
- Several beam tests
- Including irradiated samples
 - High efficiency even w/ $5x10^{14} n_{eq}/cm^2$

Lab-testbench measurement







DESY electron beam measurements



- Cross-talk from FREEZE singal prevents to achive threshold close to electrical noise level
- Bonding issues while preparing new test modules: → Currently, ~30% success rate

TJ-Monopix2 test setup in KEK



Test bench in KEK Fuji Hall B1 floor.

- Supported by KEK ITDC
- In Japan, KEK, UTokyo, ICEPP, IPMU contribute to characterisation of the TJ-Monopix2 chip.

Test in KEK PF-AR electron testbeam line

KEK PF-AR e- beam (2-5 GeV)

– New MAPS performance test hub in Japan

Tested a TJ-Monopix2 chip in the beamline on Mar 2024 as a start-up

- cluster size measurement with different incident angles
 - \rightarrow evaluate depletion layer depth











Preliminary test results



- Reasonable cluster size and charge distributions under various incident angles
- Analysis of depletion zone depth is ongoing

OBELIX prototype production

OBELIX prototype sensor (OBELIX1)



Ist OBELIX prototype sensor: OBELIX1

- All necessary functions for operation will be integrated.
- Finalizing the design now.

• OBELIX1 design ongoing: submission in late 2024

	TJ-Monopix2	OBELIX (target)
Year	2020	2024 (1st prototype)
Pixel pitch	33 µm	33 µm
Sens. area	17x17 mm ²	~30x16 mm ²
Sens. thickness	25-100 μm	~30 µm
тот	7-bit	7-bit
Integration	25 ns	25 to 100 ns
Bandwidth	320 MHz	320 MHz
Power	200 mW/cm ²	< 200 mW/cm ²
TID fluence	0.1 MGy 10 ¹⁵ n _{eq} /cm ²	< 1 MGy < 5x10 ¹⁴ n _{ec} /cm ²

iVTX Inner Layer Concept

- All-silicon module < 0.15 % X_0
 - 4 contiguous sensors diced as a block from the wafer
 - Redistribution layer for interconnection
 - Heterogeneous thinning for thinness & stiffness
- Prototyping
 - First real-size ladders at IZM-Berlin with dummy Si
 - True iVTX geometry available
- Simulation on cooling
 - Dry air cooling 15°C
 - Assume 200 mW/cm²





Demonstrator mockup with dummy Si



Metal system:

- Resistive heaters: 1.5 um Al (M1)
- 2 RDL metal layers: 3 um Cu (M2, M3)
- Top metal finish: NiAu (M4) Wirebonding, SMD soldering

Final ladder dimension: 143 x 20.4 mm²



Production finished smoothly Characterization starting

oVTX Outer Layer Concept

• Long ladders

- Evolving from ALICE-ITS2
 - Carbon-fiber truss support frame
 - Cold-plate with water coolant
 - Long-flex for power & data



- L3-4, radius 4-9 cm, length < 50 cm
 - Single sensor row, ~0.5 % X₀
- L5, radius 14 cm, length 70 cm
 - Double sensor rows , ~0.8 % X₀

Prototypes for L5 under the second sec

- Deformation & vibration
 - Max sagitta ~500 μm
 - First resonance f=250 Hz
- Signal propagation
- Cooling at T_{room} ~24°C
 - Leakless water flow at T_{in} = 10°C
 - Heaters dissipating 200 mW/cm²
 - $22^{\circ}C < T_{sensors} < 26^{\circ}C$

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Summary

CMOS DMAPS for Belle II vertex detector upgrade

- OBELIX sensor: based on TJ-Monopix2 matrix design
- Detailed performance characterization of TJ-Monopix2 is being performed for tuning OBELIX design.
 - Excellent performance is confirmed.
 - KEK and other Japanese institutes are participating in the performance test, using the KEK PF-AR electron beam facility.

• The first prototype OBELIX1 plan to be submitted in late 2024.

Mechanics design work for the VTX detector is ongoing.



Current Vertex Detector at Belle II Experiment



• VXD: Current Vertex detector in Belle II

- 2 layers of PiXel Detector (PXD): DEPFET sensor
- 4 layers of Silicon Vertex Detector (SVD): Double-sided silicon strip (DSSD) sensor SVD technical paper: arXiv:2201.09824

Roles of VXD

- Determine the vertex position
- Standalone tracking
- PID using SVD dE/dx for low p_T tracks

Performance improvement by VTX





Recovery in the tracking efficiency at future background level
 Soft pion efficiency: Factor 1.5-4.0 improvement below 75MeV/c
 B vertex resolution: ~40% better resolution

Column-Drain Readout Scheme

Toke-pass logic to read out 24-bit ToT+ToA data only from hit pixels

- Hit pixels generate tokens.
- When R/O controller finds the token, it starts reading out 24-bit data, selecting each hit pixel oneby-one using FREAZE/READ signals.





OBELIX (Optimized BELle II monolithic pIXel sensor)



• OBELIX sensor for Belle II VXD upgrade (VTX)

- Extension from TJ-Monopix2, adapting digital part for Belle II requirement
- TowerJuzz 180nm
- Ist prototype design ongoing

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HEPHY: High Energy Accelerator Research Organization. Instur Public Contract of Fisca Nuclear C



KEK PF beam test (Mar 1-4, 2024)

2 GeV e- beam

- Beam rate:
 - Counter in beamline: ~800Hz
 - Downstream scintillator (32x28mm²): ~50Hz

Tested single TJ-Monopix2 chip

- No telescope
- cluster size measurement with different incident angles
 - \bullet \rightarrow evaluate depletion layer depth









Quick results from beam test

Intensity

Entries 0001 0 14 500 - 12 400 10 disabled area disabled area disabled area 300 8 Row 6 200 4 100 - 2 0 -100 200 300 400 500 0 1000 0 Column Entries

Hit Map Distribution



ToT Distribution

DMAPS chip for Belle II vertex detector upgrade

OBELIX chip

- Optimized BELle II monolithic pIXel sensor

Pixel matrix

- Extension from TJ-Monopix2
- Clock frequency ~10-20 MHz
- Power pads
 - Power regulators added
- Periphery
 - Trigger-base readout

1st prototype: OBELIX-1

- Design & production plan
 - Designing main functionalities done (but regulator)
 - Final integration on-going
 - Simulation/verification is main activity
- Submission: expected in late 2024
 - after last in-person meeting



KEK ITDC E-sys (T. Kishishita) is contributing to designing matrix.

Column-drain readout

